Amendment to the Drawings

The attached sheets of drawings replace the original sheets of drawings including Figs. 4-5 and 6a-7c, respectively. The amendments to the drawings include changes to Fig. 4 and the addition of Fig. 6d.

The amendments to Fig. 4 include the addition of dashed line 45 indicating an optional alternative coupling of read transistor 27 to ground line 30 instead of ground line 58. Support for the alternative embodiment may be found, for example, on pages 17 and 18, lines 29-30 and line 1, respectively. Further amendments to Fig. 4 include the addition of another reference number "41" such that the conductive paths on either side of magnetic cell junction 25 are individually referenced and further to make room for dashed line 45.

Figs. 6a-6c and 7a-7c have been repositioned with respect to each other to make room for the addition of Fig. 6d on the sheet of drawings as described below.

Fig. 6d has been added to the sheet of drawings including Figs. 6a-6c and 7a-7c to illustrate an alternative configuration of the placement of conductive structure 70 with respect to magnetic cell junction 24. Support for the alternative configuration may be found, for example, on page 22, lines 23-24.

Attachment: Replacement sheets, Figs. 4-5 and 6a-7c

REMARKS

The specification and drawings have been amended for clarification purposes. In addition, claim 16 has been amended to change its claim dependency from claim 7 to claim 8 such that the claim has proper antecedent basis. As will be set forth in detail below, none of the amendments to the specification, drawings, or claim 16 introduce new subject matter. Claims 1-20 are currently pending in the case. Further examination and reconsideration of the presently claimed application is respectfully requested.

Objections to the Drawings

The drawings were objected to for not showing every feature of the invention specified in the claims. In particular, the Examiner alleges that "[c]laims 1-20 are not readable on the drawings of the present invention." In addition, the Examiner states, "Applicant is requested to particularly point out each element as recited in claims 1-20 to be read on the respective elements in the corresponding drawings of the present invention in order to help the examiner to understand the subject matter of the claim invention." As outlined in the table on the following pages, all claim limitations in claims 1-20 are illustrated in the drawings and are supported in the specification. Although it is believed that all drawings necessary for the understanding of the invention were filed in the original application, in order to expedite prosecution of the case, Fig. 4 has been amended and Fig. 6d has been added to specifically depict the limitations of claims 6 and 15.

In particular, Fig. 4 has been amended to include dashed line 45 indicating an optional alternative coupling of read transistor 27 to ground line 30 instead of ground line 58. Support for the alternative embodiment may be found, for example, on pages 17 and 18, lines 29-30 and line 1, respectively. In addition, Fig. 6d has been added to illustrate an alternative configuration of the placement of conductive structure 70 with respect to magnetic cell junction 24. Support for the alternative configuration may be found, for example, on page 22, lines 23-24. All other limitations of currently pending claims 1-20 were included in the drawings as originally filed and, thus, no further drawing amendments are believed to be necessary. The outline of support for the limitations of claims 1-20 noted below, the amendment to Fig. 4, and the addition of Fig. 6d are believed to address the concerns expressed in the Office Action and, therefore, the objection the drawings is respectfully requested.

As noted above, in addition to obliging the Examiner's request to have each element recited in claims 1-20 pointed out with the respective elements of the drawings, support for the each element recited in claims 1-20 in the specification has been cited in the table below. It is noted that the support outlined in the table not necessarily comprehensive, and, consequently, additional support may be included in the drawings and/or specification for the limitations of claims 1-20. The support noted below is, rather, outlined to help the Examiner understand the subject matter of the claims, per the Examiner's request.

Claim Limitations	Support in Drawings	Support in Specification
Claim 1: A memory cell array, comprising:	Fig. 4 - memory cell array 54	Pages 16-21
a plurality of magnetic cell junctions; and	Fig. 4 - Magnetic cell junctions 24 and 25	Page 16, lines 23-28
a first conductive line comprising:	Figs. 4 and 5 – Word line 32 or 34	Page 16, lines 26-28 (the definition of a word line as a conductive line is provided on page 12, lines 17-21)
a gate of a first transistor configured to enable a read operation for one of the plurality of magnetic cell junctions; and	Figs. 4 and 5 – Word line 32 comprises read transistor 26 and word line 34 comprises read transistor 27	Page 18, lines 7-9 and 11-14 (the definition of a read transistor is provided on page 10, lines 4-7)
a gate of a second transistor configured to enable a write operation for another of the plurality of magnetic cell junctions.	Figs. 4 and 5 – Word line 32 comprises program transistor 29 and word line 34 comprises program transistor 28	Page 18, lines 9-14 (the definition of a program transistor is provided on page 10, lines 11-13)
Claim 2: The memory cell array of claim 1, wherein the gate of the first transistor is one of a plurality of gates within the first conductive line configured to enable read operations for a first set of the magnetic cell junctions, and wherein the gate of the second transistor is one of a plurality of gates within the first conductive line configured to enable write operations for a second set of the magnetic cell junctions.	Fig. 4 – The continuation dots to the around the portion of memory array 54 shown indicate additional memory cells may be included in the memory array having similar configurations as memory cells 22a-22d.	Page 8, lines 13-18 and Page 18, lines 14-17
Claim 3: The memory cell array of claim 2, wherein the gates configured to enable read operations for the first set of the	Fig. 4 – The continuation dots to the around the portion of memory array 54	Page 18, lines 17-18

Claim Limitations	Support in Drawings	Support in Specification
magnetic cell junctions and the gates configured to enable write operations for the second set of the magnetic cell junctions are alternately arranged within the first conductive line.	shown indicate additional memory cells may be included in the memory array having similar configurations as memory cells 22a-22d.	
Claim 4: The memory cell array of claim 1, further comprising a second conductive line comprising: a gate of a third transistor configured to enable a write operation for the magnetic cell junction having a read operation enabled by the first transistor; and a gate of a fourth transistor configured to enable a read operation for the magnetic cell junction having a write operation enabled by the second transistor.	Figs. 4 and 5 – Word line 32 or 34 (depending on which word line is referenced as the first conductive line in claim 1) Figs. 4 and 5 – Word line 32 comprises read transistor 26 and program transistor 29; Word line 34 comprises read transistor 27 and program transistor 28	Page 16, lines 26-28 Page 18, lines 7-14
Claim 5: The memory cell array of claim 4, wherein the second and third transistors are coupled to a common program line.	Fig. 4 – Program transistors 28 and 29 are coupled to program line PROG0	Page 19, line 9-10
Claim 6: The memory cell array of claim 4, wherein the first and fourth transistors are coupled to a common ground contact.	Fig. 4 – Read transistors 26 and 27 are optionally coupled to ground contact 30 by dashed line 45	Pages 17 and 18, lines 29-30 and 1-3, respectively.
Claim 7: The memory cell array of claim 4, wherein the first and second conductive lines are coupled to a common word line.	Fig. 4 – Word lines 32 and 34 are coupled to global word line 56	Page 20, lines 7-10
Claim 8: A memory cell array, comprising: a magnetic cell junction; a bit line spaced apart from the magnetic cell junction;	Figs. 1 and 4 – memory arrays 20 and 54 Figs. 1 and 4 – magnetic cell junction 24 Figs. 7b and 7c – bit line BLO spaced above magnetic cell junction 24	Pages 8-21 Page 9, line 24; Page 16, lines 23-28; Page 30, lines 12-16. In addition, page 30, lines 17-19 clearly state the configurations

Claim Limitations	Support in Drawings	Support in Specification
		depicted in Figs. 7a-7c may be employed within memory array 20, 52, or 54.
a first set of conductive structures serially coupled to the bit line, wherein one or more of the first set of conductive structures are configured to induce a magnetic field about the magnetic cell junction;	Figs. 1 and 4 – conductive line 36 and conductive path 40 Fig. 7b – vias 84 and 74, and conductive structures 70 and 72	Pages 9 and 10, lines 25-30 and lines 7-9. Page 31, lines 1-9
a transistor coupled to the first set of conductive structures; and	Figs. 1 and 4 – program transistor 28	Page 10, lines 9-13
a program line collectively configured with the bit line to induce current flow through the first set of conductive structures upon an application of a voltage to a gate of the transistor.	Figs. 1 and 4 – program line PROG0 configured with bit line BL0 to induce current flow through magnetic cell junction 24 upon application of voltage to a gate of program transistor 28	Page 4, lines 18-22
Claim 9: The memory cell array of claim 8, wherein the program line is further configured, with a different bit line, to induce current flow through a second set of conductive structures arranged adjacent to a different magnetic cell junction of the array upon an application of a voltage to a gate of a different transistor.	Fig. 4 – program line PROG0 configured with bit line BL1 to induce current flow through magnetic cell junction 25 upon application of voltage to a gate of program transistor 29	Page 5, lines 11-15
Claim 10: The memory cell array of claim 8, wherein the first set of conductive structures comprises at least two segments respectively aligned with opposing sides of the magnetic cell junction.	Figs. 7b and 7c – conductive structures 70 and 72	Page 5, lines 1-2
Claim 11: The memory cell array of claim 10, wherein the first set of conductive structures comprises a third segment connecting the at least two segments.	Fig. 7b – via 74	Page 5, lines 2-3
Claim 12: The memory cell array of claim 10, wherein the at least two segments are arranged parallel to each other.	Figs. 7a-7c	Page 5, line 4

Claim Limitations	Support in Drawings	Support in Specification
Claim 13: The memory cell array of claim 12, wherein the magnetic cell junction is configured to have an easy axis arranged at an angle between approximately 0° and approximately 90° relative to the two segments.	Fig. 7a	Page 29, lines 15-17; Page 30, lines 21-23
Claim 14: The memory cell array of claim 10, wherein at least one of the two segments is arranged in contact with the magnetic cell junction.	Figs. 7b and 7c – conductive structure 70	Page 22, lines 21-22; Page 30, lines 21-23
Claim 15: The memory cell array of claim 10, wherein at least one of the two segments is electrically connected to the magnetic cell junction through a via.	Fig. 6d – conductive structure 70	Page 22, lines 23-24; Page 30, lines 21-23
Claim 16: The memory cell array of claim 8, wherein the bit line is spaced directly above the magnetic cell junction.	Figs. 7a and 7c – bit line BLO is spaced directly above magnetic cell junction 24	Page 31, lines 13-14
Claim 17: A memory array, comprising:	Figs. 1, 3, and 4 – memory arrays 20, 52, and 54	Pages 8-21
a plurality of magnetic cell junctions;	Figs. 1, 3, and 4 – magnetic cell junctions (mcj) 24 in Fig. 1, mcj 24a and 24b in Fig. 3 and mcj 24 and 25 in Figs. 4a and 4b	Page 9, lines 6-24; Page 15, lines 20-28; Page 16, lines 26-28; Page 17, lines 13-14;
a bit line spaced above and arranged in vertical alignment with the plurality of magnetic cell junctions; and	Figs. 7b and 7c – bit line BLO spaced above and in vertical alignment with magnetic cell junction 24	Page 30, lines 12-16. In addition, page 30, lines 17-29 clearly state the configurations depicted in Figs. 7a-7c may be employed within memory array 20, 52, or 54.
a series one or more conductive structures coupled between the bit line and one of the plurality of magnetic cell junctions.	Figs. 1, 3, and 4 – conductive line 36 and portions of conductive path 40 (40a and 40b in Fig. 3); Fig. 7b – via 84 and conductive structure 70	Page 22, lines 21-24; Page 30, lines 21-25; Page 31, line 9
Claim 18: The memory array of claim 17, wherein the series of one or more conductive structures is configured to	Figs. 1, 3, and 4 – conductive line 36 and conductive path 40 (40a and	Pages 9 and 10, lines 25-30 and lines 7-9.

Claim Limitations	Support in Drawings	Support in Specification
induce a magnetic field about the magnetic cell junction.	4b in Fig. 3); Fig. 7b – vias 84 and 74, and conductive structures 70 and 72	Page 31, lines 1-5
Claim 19: The memory array of claim 17, further comprising:		
a transistor coupled to the series of one or more conductive structures; and	Figs. 1 and 4 – program transistor 28	Page 10, lines 9-13
a program line collectively configured with the bit line to induce current flow through the series of one or more conductive structures upon an application of voltage to a gate of the transistor.	Figs. 1, 4a, and 4b – program line PROG0	Page 4, lines 18-22
Claim 20: The memory array of claim 17, wherein the series of one or more conductive structures is one of a plurality of sets of serially connected conductive structures coupled between the bit line and the plurality of magnetic cell junctions.	Figs. 1 and 4 – conductive structure 36 and conductive path 40 coupled to bit line BL0 in memory cells 22a and 22c	Page 9, lines 6-9

Section 112, 2nd Paragraph Rejection

Claims 1-20 were rejected under 35 U.S.C. § 112, second paragraph, for failing to particularly point out and distinctly claim the subject matter the applicant regards as the invention. In particular, the Examiner states that he/she does not understand the subject matter of the claims 1, 2, 4, and 17-20. The following addresses the particular issues noted in the Office Action which appear to be contributing to his/her confusion.

The Examiner states on page 3 of the Office Action that "it is not clear how a first conductive line can comprise a gate of a first transistor and a gate a second transistor." The Examiner issues a similar statement for the limitations of claim 4 in which a second conductive line is recited having gates of two different transistors. In an effort to explain such a configuration, the Examiner's attention is directed at Fig. 5. Fig. 5 outlines a top view of a microelectronic topography detailing a configuration of conductive lines and adjacent diffusion and isolation regions, which collectively define a plurality of transistors. In particular, Fig. 5 illustrates word lines 32 and 34 spanning over isolation strictures 64 and 66 and diffusion regions 60 and 62, defining transistors 26-29. The portions of word lines 32 and 34 over

diffusion regions 60 and 62 serve as the gates of the transistors, the portions of diffusion regions 60 and 62 on opposing sides of the word lines serve as source and drain regions of the transistors, and the portions of isolation structures 64 and 66 between diffusion regions 60 and 62 isolate the transistors, distinguishing them as distinct devices. As such, word line 32 includes gates of transistors 26 and 29 and word line 34 includes gates of transistors 27 and 28. Consequently, the language of claims 1 and 4 is definite.

The Examiner further states in relation to the limitations of claims 1, 2, and 4 that the connective relationship of the magnetic cell junctions, the first/second conductive line, and the first-fourth transistors is not defined. As noted above, the concept of how conductive lines may include gates of different transistors is well described in the specification, clearly illustrated in the drawings, and is clearly pointed out and distinctly defined in claims 1 and 4. In addition, the connectivity of the first and second conductive lines and gates of the transistors to the magnetic cell junctions is clearly outlined in the drawings, specification, and claims. In particular, the drawings and the corresponding text of the specification show/describe transistors along word lines of memory arrays coupled to conductive paths arranged around and through magnetic junctions such that read and write operations of the magnetic cell junctions may be performed. In addition, claims 1 and 4 recite the functionality of the transistors to enable the read and write operations of the magnetic cell junctions. In other words, claims 1 and 4 recite the connectivity of the transistors with respect to the magnetic cell junctions in terms of the function the transistors relative to the magnetic cell junctions. Claim 2 specifies the first conductive line includes gates of a plurality transistors for enabling read operations of a set of magnetic cell junctions as well as gates of another plurality transistors for enabling write operations of a different set of magnetic cell junctions. Such a limitation is supported by the description in the Specification stating that word lines 32 and 34 may extend along additional memory cells and have similar configurations as described for those depicted in the figures. As such, it is asserted that the connective relationship of the magnetic cell junctions, the first/second conductive line, and the first-fourth transistors is defined in claims 1, 2, and 4.

The Examiner states on page 3 of the Office Action in relation to claims 17-20 that "it is not clear what the conductive structures really are." As noted above in the table providing support for the limitations of claims 1-20, reference to what conductive structures coupled between a bit line and one of a plurality of magnetic cell junctions (as recited in claim 17) are is clearly shown in the drawings and described in the specification. In particular, Figs. 1, 3 and 4

are shown and described as having conductive line 36 and conductive path 40 interposed between bit line BLO and magnetic cell junction 24. In addition, Fig. 7b is shown and described as having via 84 and conductive structure 70 disposed therebetween. As such, reference to what the conductive structures recited in claims 17-20 are is clear.

The Examiner further states the term "about" in claim 18 is vague and indefinite. Merriam-Webster's Dictionary defines the term "about" as 'in a circle around, on every side of, around'. As such, the use of the term within claim 18 clearly refers to the arrangement of the magnetic field around the magnetic cell junction. It is asserted that those skilled in the art are aware of the term "about" and the characteristics of an induced magnetic field to encircle a structure including magnetic materials. As such, the term "about" within clam 18 is neither vague nor unclear.

As set forth above, the language in claims 1, 2, 4, and 17-20 is clear and definite, setting the metes and bounds of the subject matter recited therein. In addition, it is asserted that claims 3 and 5-16 are definite as well. Consequently, removal of the § 112, second paragraph rejection of claims 1-20 is respectfully requested.

Section 103 Rejection

Claims 1-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable by U.S. Patent No. 6,639,831 to Pancholy et al. (hereinafter referred to as "Pancholy"). As described in a previous reply to the Office Action dated May 4, 2005 in the captioned case, Pancholy fails to anticipate the limitations of claims 1-20. The Examiner acknowledges such a lack of teaching on page 4 of the Office Action. The Examiner, however, disregards such a lack of teaching stating the limitations of claims 1-20 missing in Pancholy are vague and indefinite (as rejected under the second paragraph of 35 U.S.C. § 112) and, therefore, are obvious. First of all, such a basis for rejection is improper. In particular, it has been noted in previous case law that if no reasonably definite meaning can be ascribed to certain claim language, the claim is indefinite, not obvious. *In re Wilson*, 424 F. 2d 1382, 165 USPQ 494 (CCPA 1970) MPEP 2143.03. Since the Examiner was not able to ascertain a definite meaning of the language in claims 1-20 (as noted in the 35 U.S.C. § 112, second paragraph rejection of the claims), no obvious type rejection of the claims can be rendered. Accordingly, removal of the § 103(a) rejection of claims 1-20 is respectfully requested.

As noted above, the language of claims 1-20 is clear and definite and the Examiner is requested to examine the claims in regard thereto. The Examiner is reminded that Pancholy does not teach or suggest a memory array with a conductive line having different transistor gates configured to respectively enable read and write operations for different magnetic cell junctions of the memory array (as noted in the reply to the Office Action dated May 4, 2005). In addition, Pancholy does not teach or suggest a memory array with a bit line spaced apart from a plurality of magnetic cell junctions and further with a series one or more conductive structures coupled between the bit line and one of the plurality of magnetic cell junctions (as noted in the reply to the Office Action dated May 4, 2005). Without any teach or suggestion of such limitations, there is no motivation for one skilled in the art to create the memory arrays recited in claims 1-20 in light of Pancholy. As such, claims 1-20 are patentably distinct from Pancholy.

CONCLUSION

This response constitutes a complete response to the issues raised in the Office Action mailed September 19, 2005. In view of the remarks traversing the rejections, Applicants assert that pending claims 1-20 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees, which may be required, or credit any overpayment, to Daffer McDaniel LLP Deposit Account No. 50-3268/5298-17000.

Respectfully submitted,

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